FIG.1

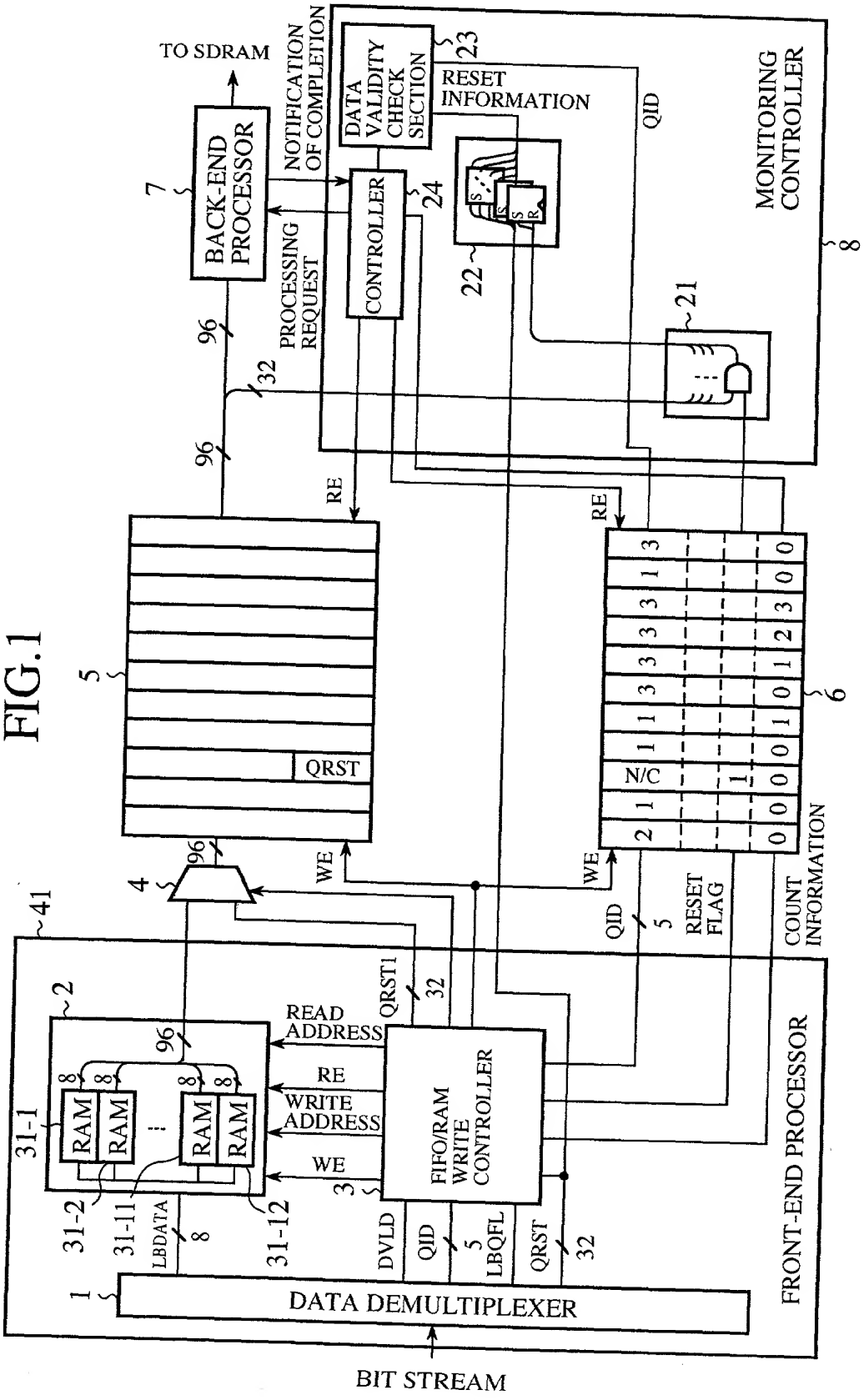
TO SDRAM
BACK-END PROCESSOR
7
NOTIFICATION OF COMPLETION
PROCESSING REQUEST
DATA VALIDITY CHECK SECTION
23
RESET INFORMATION
QID
CONTROLLER
24
22
21
MONITORING CONTROLLER
8
96
32
96
RE
RE
5
QRST
6
N/C
4
96
WE
WE
41
QID
5
RESET FLAG
COUNT INFORMATION
2
QRST1
32
READ ADDRESS
RE
WRITE ADDRESS
WE
3
FIFO/RAM WRITE CONTROLLER
96
8
RAM
31-1
31-2
31-11
31-12
LBDATA
8
DVLD
QID
5
LBQFL
QRST
32
1
DATA DEMULTIPLEXER
FRONT-END PROCESSOR
BIT STREAM

FIG.2

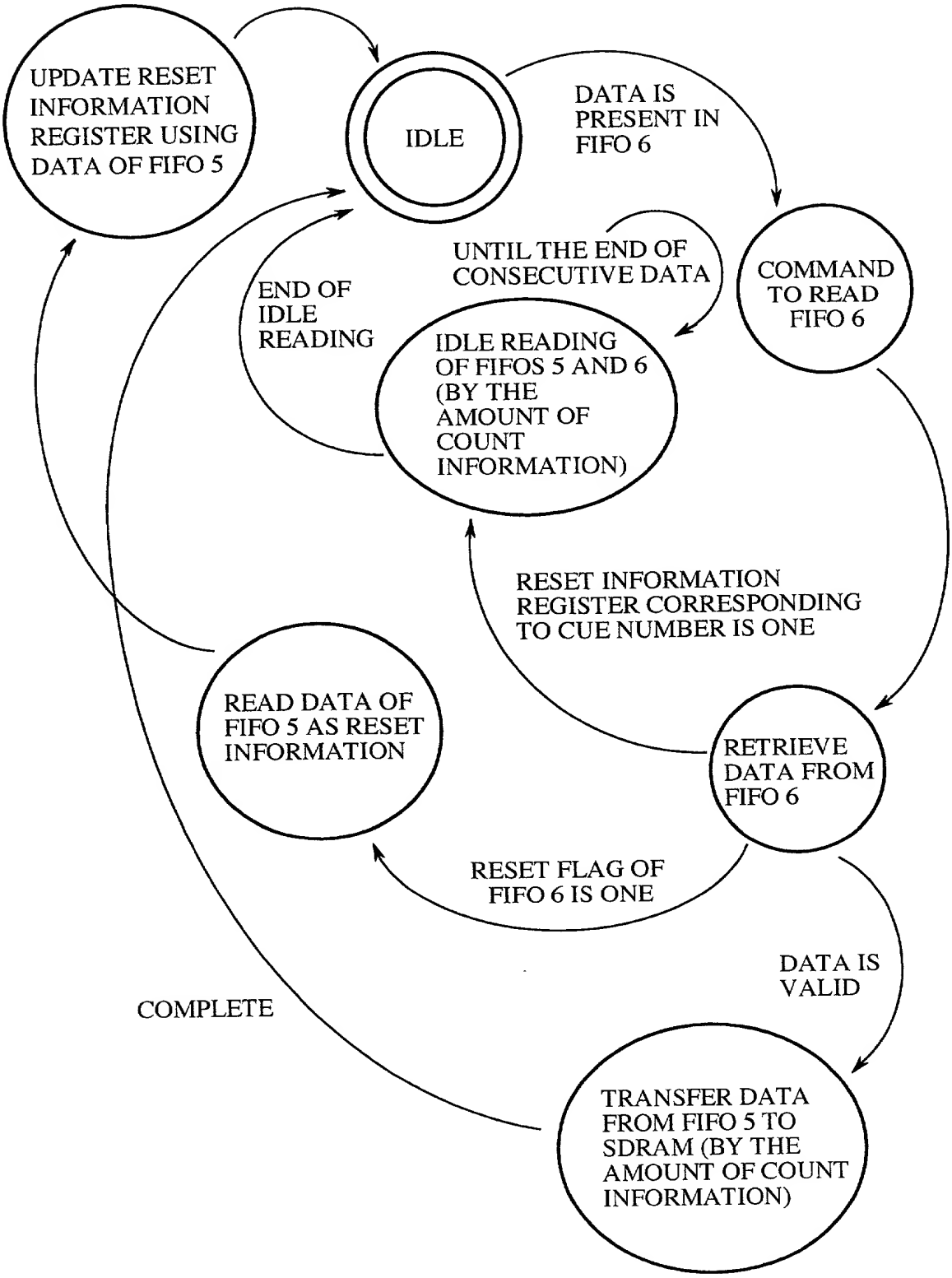
UPDATE RESET INFORMATION REGISTER USING DATA OF FIFO 5
IDLE
DATA IS PRESENT IN FIFO 6
COMMAND TO READ FIFO 6
UNTIL THE END OF CONSECUTIVE DATA
END OF IDLE READING
IDLE READING OF FIFOS 5 AND 6 (BY THE AMOUNT OF COUNT INFORMATION)
RESET INFORMATION REGISTER CORRESPONDING TO CUE NUMBER IS ONE
READ DATA OF FIFO 5 AS RESET INFORMATION
RETRIEVE DATA FROM FIFO 6
RESET FLAG OF FIFO 6 IS ONE
DATA IS VALID
COMPLETE
TRANSFER DATA FROM FIFO 5 TO SDRAM (BY THE AMOUNT OF COUNT INFORMATION)

FIG.3

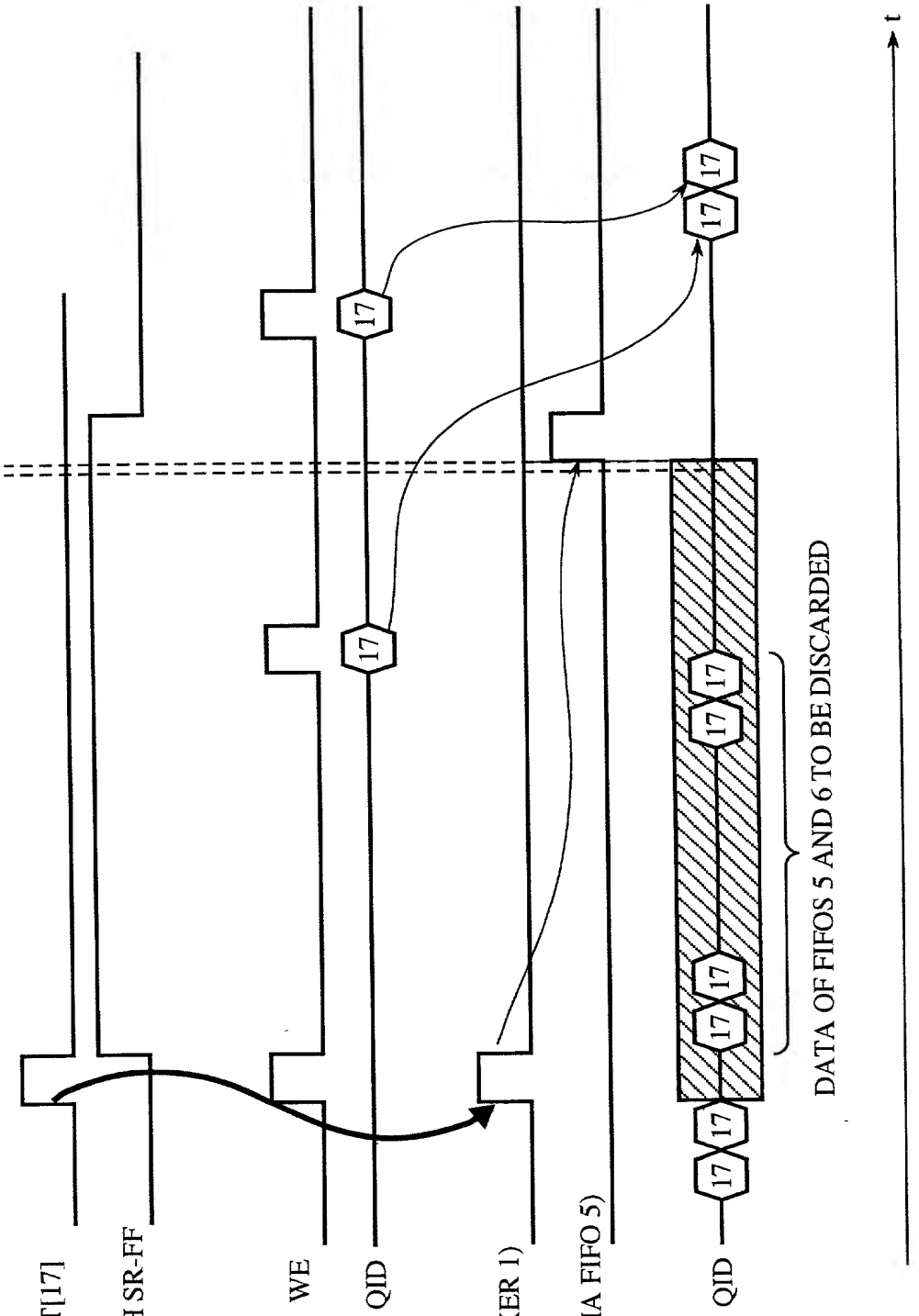
LBQRST[17]
VALUE OF 17TH SR-FF
WE
QID
RESET FLAG (VIA DATA DEMULTIPLEXER 1)
RESET FLAG (VIA FIFO 5)
QID
17
DATA OF FIFOS 5 AND 6 TO BE DISCARDED
t

FIG.4

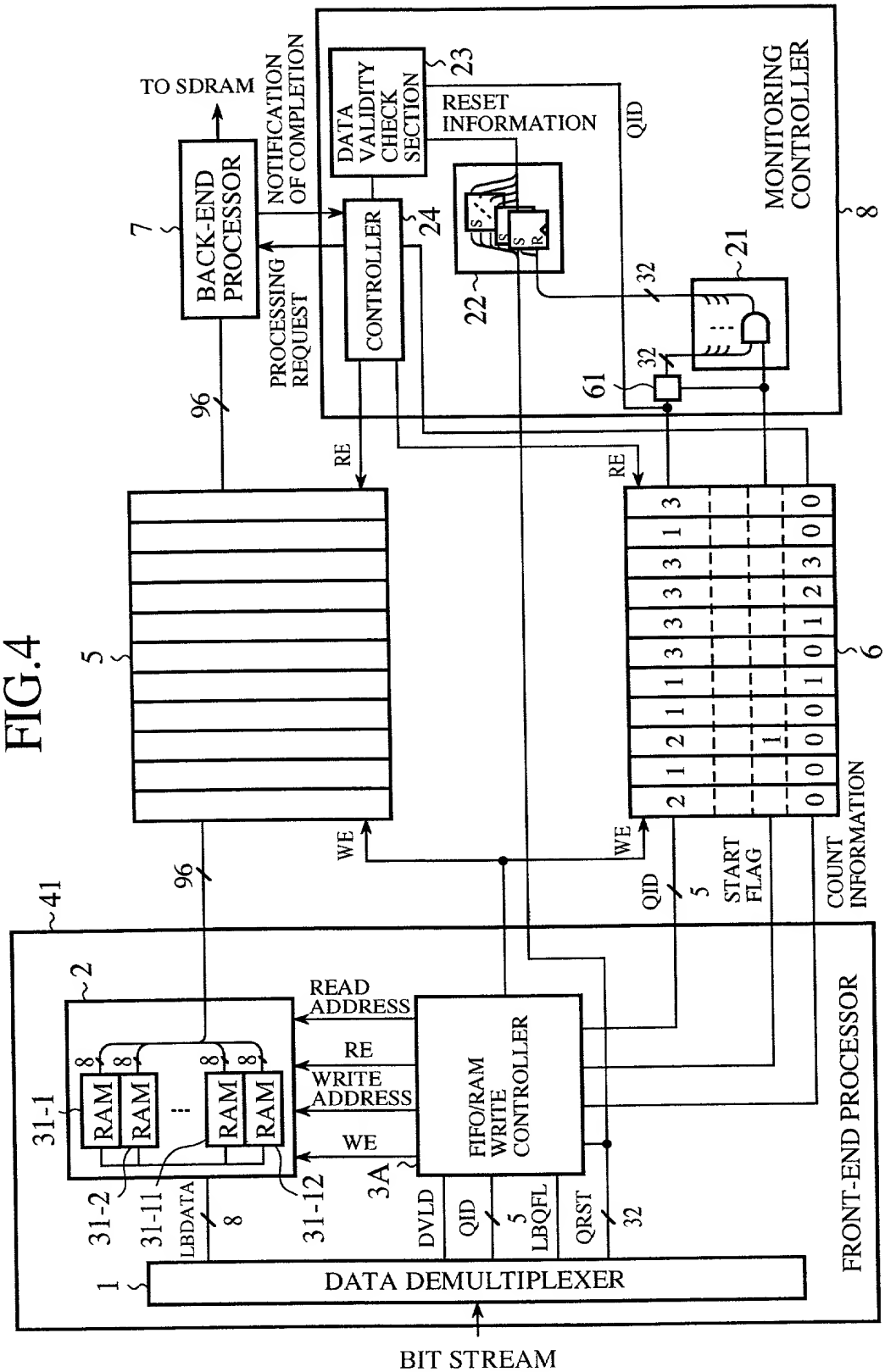
TO SDRAM
BACK-END PROCESSOR
7
NOTIFICATION OF COMPLETION
PROCESSING REQUEST
CONTROLLER
24
DATA VALIDITY CHECK SECTION
23
RESET INFORMATION
QID
MONITORING CONTROLLER
8
22
21
32
61
96
RE
WE
5
6
START FLAG
COUNT INFORMATION
41
2
31-1
31-2
31-11
31-12
RAM
READ ADDRESS
RE
WRITE ADDRESS
WE
3A
FIFO/RAM WRITE CONTROLLER
LBDATA
DVLD
QID
LBQFL
QRST
1
DATA DEMULTIPLEXER
FRONT-END PROCESSOR
BIT STREAM

FIG.5

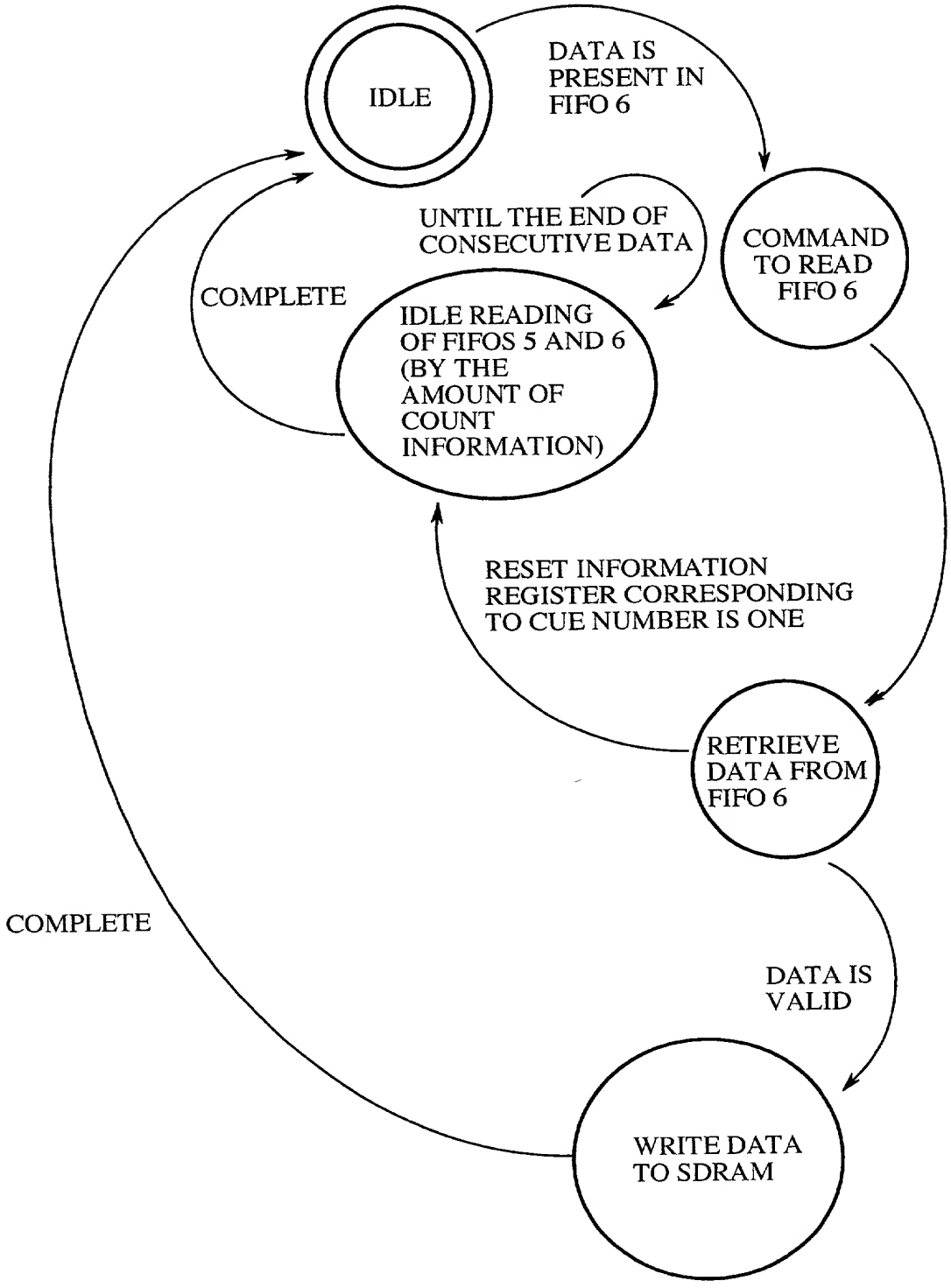
IDLE
DATA IS PRESENT IN FIFO 6
COMMAND TO READ FIFO 6
UNTIL THE END OF CONSECUTIVE DATA
COMPLETE
IDLE READING OF FIFOS 5 AND 6 (BY THE AMOUNT OF COUNT INFORMATION)
RESET INFORMATION REGISTER CORRESPONDING TO CUE NUMBER IS ONE
RETRIEVE DATA FROM FIFO 6
COMPLETE
DATA IS VALID
WRITE DATA TO SDRAM

FIG.6

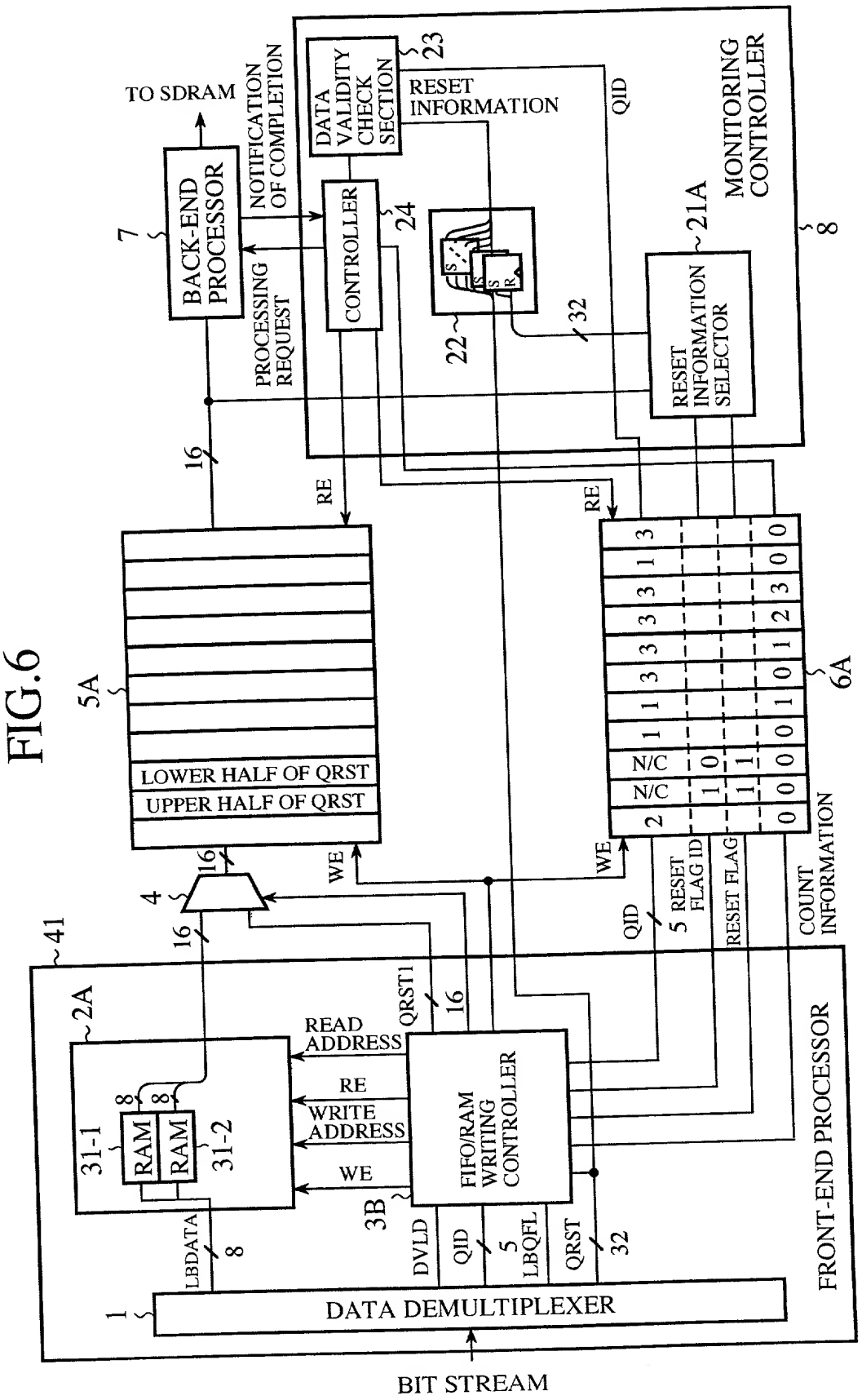
TO SDRAM
BACK-END PROCESSOR
7
NOTIFICATION OF COMPLETION
PROCESSING REQUEST
DATA VALIDITY CHECK SECTION
23
RESET INFORMATION
QID
CONTROLLER
24
22
32
RESET INFORMATION SELECTOR
21A
MONITORING CONTROLLER
8
16
RE
5A
LOWER HALF OF QRST
UPPER HALF OF QRST
4
WE
6A
N/C
N/C
RESET FLAG ID
RESET FLAG
COUNT INFORMATION
5
41
2A
31-1
RAM
RAM
31-2
READ ADDRESS
RE
WRITE ADDRESS
WE
QRST1
FIFO/RAM WRITING CONTROLLER
3B
DVLD
QID
LBQFL
QRST
LBDATA
DATA DEMULTIPLEXER
FRONT-END PROCESSOR
BIT STREAM

FIG.7

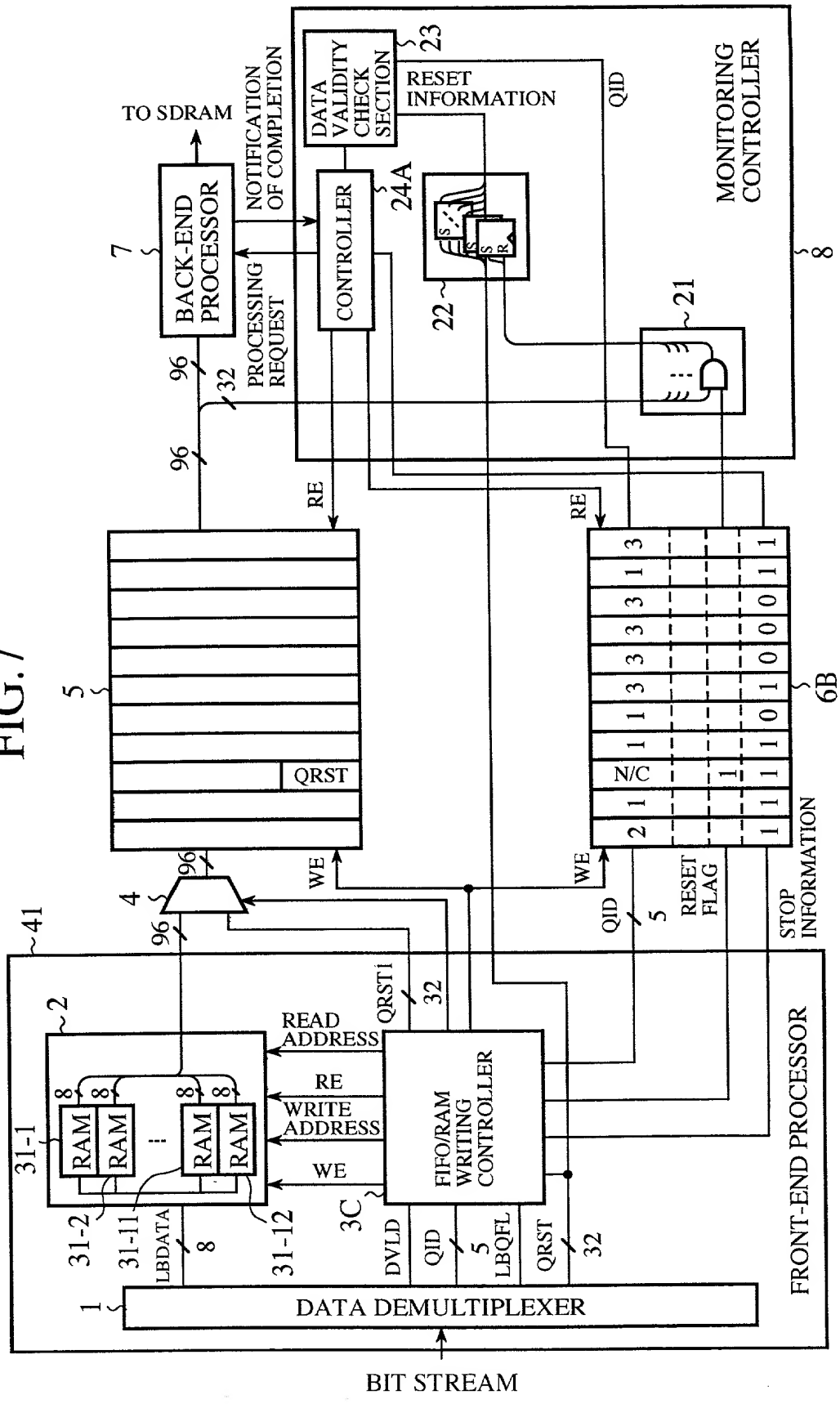
TO SDRAM
BACK-END PROCESSOR
7
NOTIFICATION OF COMPLETION
PROCESSING REQUEST
DATA VALIDITY CHECK SECTION
23
RESET INFORMATION
QID
CONTROLLER
24A
22
21
MONITORING CONTROLLER
8
96
32
RE
5
QRST
6B
N/C
WE
4
41
2
QRST1
READ ADDRESS
RE
WRITE ADDRESS
WE
FIFO/RAM WRITING CONTROLLER
3C
RAM
31-1
31-2
31-11
31-12
LBDATA
DVLD
QID
LBQFL
QRST
RESET FLAG
STOP INFORMATION
FRONT-END PROCESSOR
1
DATA DEMULTIPLEXER
BIT STREAM

FIG.8 (PRIOR ART)